according to the first time and pulling down a word line to avoid further current sinking through the memory cell; and

a delay device for controlling a second time to discharge a bit line and a bit line-bar of the memory array;

Claim 9. (Cancelled)

Remarks and Responses

Claim 1 has been amended. Support for the amendments is found in the specification of page 11, paragraph 2, Fig. 4 depicts the circuit according to the present invention of a low power and low noise sensing scheme. Two N-type devices 41, 42 discharge the bit line 43 and bit line-bar 44 all the way down to ground after data accessing operation is done. During the accessing period, one of the two P-type transistors 451, 452 of the memory cell 45 pulls the bit line 43 or bit line-bar 44 voltage level up to differentiate the voltage difference between bit line and the bit line-bar which is also the differential voltage input to the sense amplifier.

Claim 9 is added to Claim 8 and cancelled. Accordingly, the amendments do not constitute the addition of new matter. Reconsideration of the application in view of the foregoing amendments and following comments is respectfully requested.

The specific changes to the amended claims are shown on a separate set of pages attached hereto and entitled LOW POWER SENSING SCHEME FOR THE SEMICONDUCTOR MEMORY, which follows the signature page of this Amendment.

Objections for Claims 9-14

With respect to paragraph 2 of the Office Action, the Examiner regards that Claims 9-14 are allowable in view of prior art.

Applicant amends independent Claim 8 by adding limitations from Claim 9 thereto. Accordingly, reconsideration and withdrawal of this objection is respectfully requested.

Claim Rejection - 35 U.S.C. § 102

With respect to Paragraphs 3-5 of the Office Action, the Examiner rejected Claims 1-7 under 35 U.S.C. § 102 (b) as being anticipated by Kumagai et al. U.S. Patent No. 6,255,862. Of the rejected claims, only Claim 1 is independent.

Applicant respectfully traverses this rejection as well as the cited patent. In Kumagai et al. U.S. Patent No. 6,255,862, pulling up bit-line an bit-bar to VDD same like most other alternatives during non-accessing cycle; pulling down by memory cell, said SRAM during accessing cycle.

Besides, when applying 35 U.S.C. § 102, the following tenets of patent law must be adhered to:

> **"A claim is anticipated only if <u>each and every element</u> as set forth in the claim is found, either expressly or inherently described, <u>in a single prior art reference</u>."** *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in <u>as complete detail as</u> is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). (MPEP §2131)

With respect to amended Claim 1, Kumagai et al. do not disclose discharging the bit-line and bit-bar to ground during non-accessing cycle. Kumagai et al. do not disclose pulling up the bit and bit-bar by P-MOS during accessing mode, either. In conclusion, Kumagai et al. do no disclose elements as set forth in Claim 1. Since Kumagai et al. do not show as complete details as contained in Claim 1, Claim 1 should have novelty when compared with Kumagai et al. .

Accordingly, Applicant respectfully submits that independent Claim 1 as amended is allowable over the art of record and respectfully requests the 35 U.S.C. § 102 (b) rejection of Claim 1 to be reconsidered and withdrawn. In addition, insofar claims 2-4, 6, 8-9 depend from independent Claim 1 and add further limitations thereto, the 35 U.S.C. § 102 (b) rejection of these claims should be withdrawn as well.

Reconsideration and withdrawal of this rejection is respectfully requested.

Nonobviousness of Claims 1-7

In addition to novelty, amended Claim 1 is nonobvious in view of Kumagai et al. What Kumagai et al. are applying to sensing scheme with pulling up bit-line and bit-bar when non-accessing, and pulling down bit-line and bit-bar through memory cell when in accessing. In contrast, amended

Claim 1 recites pulling down bit-line and bit-bar when non-accessing through N-type devices, and pulling up bit-line and bit-bar through memory cell when in accessing.

Besides, when applying 35 U.S.C. § 103, the following tenets of patent law must be adhered to:

(A) The claimed invention must be **considered as a whole**;

(B) The references must be considered as a whole and must **suggest the desirability** and thus the obviousness of making the combination;

(C) The references must be **viewed without the benefit of impermissible hindsight vision afforded by the claimed invention** and

(D) **Reasonable expectation of success** is the standard with which obviousness is determined.

Hodosh v. Block Drug Co., Inc., 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986). (MPEP §2141)

In view of above, amended Claim 1 is nonobvious in view of Kumagai et al. Claims 2-7 add further limitations to Claim 1 and should be nonobvious in view of Kumagai et al., too.

Accordingly, applicant respectfully submits that all Claim 1-7 and 10-14 should have patentability.

Reconsideration and withdrawal of this rejection is respectfully requested.

Other cited references of record have been studied, and are found no more relevant to the present invention than the applied art.

All claims in the present application are now in condition for allowance. Early and favorable indication of allowance is courteously solicited.

Conclusions

For all of the above reasons, applicants submit that the claims are now in proper form, and that the claims define patentable over the prior art. Therefore applicants respectfully request the Examiner to pass the case to issue at the earliest convenience.

Respectfully submitted,

May. 18th. 2005

Chih-Ta Star Sung

Applicant/Inventor

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

1. (Amended) A semiconductor memory sensing circuit in a memory array, comprising:

at lease one memory cell of a memory array, that generates a first voltage output and a second voltage output when the memory cell is accessed, wherein the first voltage output ramps from a predetermined voltage level to a higher voltage level, and the second voltage output keeps in a predetermined voltage level;

a first N-type device coupled between ground and one corresponding bit line of the memory array, wherein discharging the bit line voltage when memory array accessing is completed;

a second N-type device coupled between ground and one corresponding bit line-bar of the memory array, wherein discharging the bit line voltage when memory array accessing is completed; ; and

a differential amplifier with two input nodes coupled to the bit line and the bit line-bar of the memory array to generate a first sense output voltage if the first voltage output of one memory cell is higher than a second voltage output of the one memory cell and to generate a second sense output

voltage if the first voltage output of one memory cell is lower than a second voltage output of the one memory cell.

2. The circuit as recited in claim 1, wherein the memory cell has at least one semiconductor device.

3. The circuit as recited in claim 1, wherein the memory cell has a static random access memory (SRAM) device.

4. The circuit as recited in claim 3, wherein the SRAM cell has at least one back-to-back inverting circuit with both inverting devices hooked up to VDD through a pull-up device and to Ground through a pull-down device.

5. The circuit as recited in claim 4, wherein the pull-up device has a P-type semiconductor device and the pull-down device has an N-type semiconductor device.

6. The circuit as recited in claim 4, wherein the pull-up device has a resistor and the pull-down device has another resistor.

7. The circuit as recited in claim 1, wherein the differential amplifier has an amplifier circuit with at least two differential input nodes and a control input for enabling and disabling the amplifier circuit.

8. (Amended) A control circuit for a semiconductor memory array, comprising:

a sense amplifier for amplifying output from a memory cell;

a self-timer coupled to the sense amplifier for counting a time and sending out control signals to shut off the sense amplifier according to the time and pulling down a word line to avoid further current sinking through the memory cell; and

a delay device for controlling a second time to discharge a lit line and a bit line-bar of the memory array

9. (Cancelled)

9. The circuit as recited in claim 8, wherein the self-timer counts the time of differentiating a voltage between the bit line and the bit line-bar.

10 The circuit as recited in claim 8, wherein when the differential

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voltage of the bit line and the bit line-bar reaches a predetermined threshold, the self-timer sends a signal to turn off the word line.

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11. The circuit as recited in claim 8, wherein when the differential voltage of the bit line and the bit line-bar reaches a predetermined threshold, the self-timer sends a signal to enable the sense amplifier.

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12. The circuit as recited in claim 9, wherein when the differential voltage of the bit line and the bit line-bar reaches a predetermined threshold, the delay device send a signal to discharge the bit line and bit line-bar.

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13. The circuit as recited in claim 9, wherein the delay device postpones the time and sends a signal to turn on N-type devices to discharge the bit line and bit line-bar to avoid overlapping of the word line and the bit line and bit line-bar.